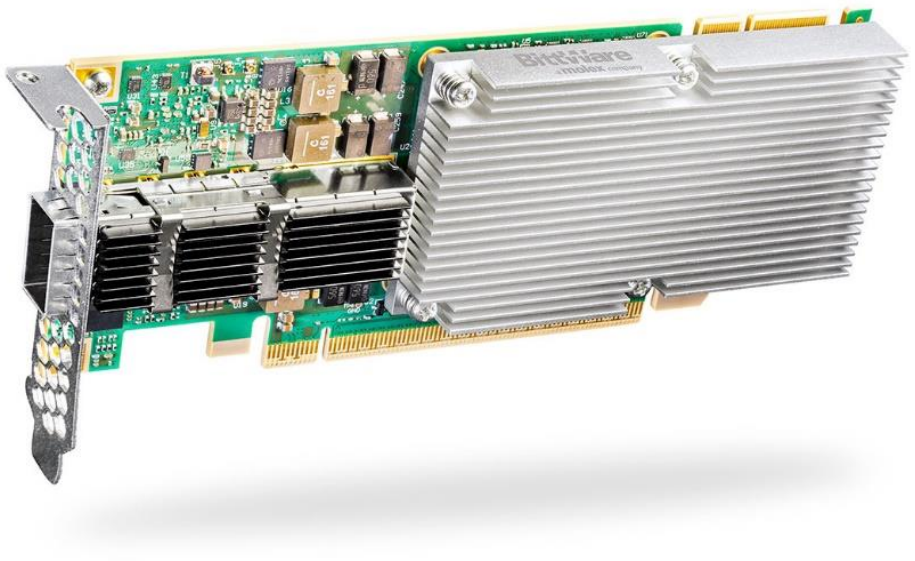

IA-440i

Hardware Reference Guide

BittWare
a molex company

IA-440i
Hardware Reference Guide

Document Revision: 11/14/2023
Hardware Revision: 0

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Country of Origin

The IA-440i's Country of Origin is the United States of America.

Compliance

Compliance testing is currently in progress for this FPGA card.

Contents

1 Introduction

1.1 About this Guide

This Hardware Reference Guide describes the components and interfaces on the Rev. 0 IA-440i.

1.2 Revision History

1.2.1 Board Revisions

The table below lists the hardware revisions for the IA-440i and the differences between them.

Table 1 Hardware revisions

Release Date	Hardware Revision	Notes/Changes
3-Apr-2023	0	Early Access Unit release

1.2.2 Document Revisions

The table below lists the revision history of this document.

Table 2 Document revisions

Release Date	Document Revision	Notes/Changes
23-May-2023	0.0	Early Access Unit release
14-Nov-2023	1.0	Updated for AGIB023R18A1E1V devices and hardware Rev 1 release

1.3 Related Documentation

Refer to the following documents (available on the BittWare developer site) for more information about the IA-440i:

- IA-440i Getting Started Guide
- IA-440i BMC Reference Guide
- IA-440i FPGA Developer Reference Guide
- IA-440i SDK and CSP Reference Guide
- Intel Agilex FPGA documentation
- Intel Channel Placement Tools (for E-Tile and F tile)

1.4 Abbreviations & Definitions

- BMC Board Management Controller
- CSP Card Support Package
- CvP Configuration Via Protocol
- DDR Double Data Rate
- FPGA Field Programmable Gate Array

- Gb Gigabit
- GB Gigabyte
- I2C Inter-IC bus (standard)
- IO Input/Outputs
- IP Intellectual Property
- JTAG Joint Test Action Group (boundary scan standard)
- LED Light Emitting Diode
- MCTP Management Component Transfer Protocol
- MT/s Mega Transfers per second
- PLDM Platform Level Data Model
- POF Programmer Object File
- PR Partial Reconfiguration
- QSFP Quad Small Form-factor Pluggable
- QSFP-DD QSFP Double Density
- SDRAM Synchronous Dynamic Random-Access Memory
- SOF SRAM Object File
- SPI Serial Peripheral Interface
- PROM Programmable Read-Only Memory
- QSPI Quad Serial Peripheral Interface
- TCXO Temperature Compensated Xtal (crystal) Oscillator
- VID Voltage IDentification

1.5 Contacting BittWare

BittWare is dedicated to providing customers with superior technical support:

- **BittWare Developer Site:** The BittWare Developer Site provides online access to our technical support resources. Go to developer.bittware.com to register for an account. Once you have set up an account, you will have access to BITTS (the BittWare Issue Tracking and Technical Support site), BittWare product documentation, software downloads, release notes, and examples. When you are logged into the Developer Site, follow the "Issue Tracking" link at the top right of the screen to access BITTS.
- **BittWare's website:** Our website at www.bittware.com provides a variety of literature, including whitepapers, datasheets, and articles.
- **Phone**: You can also call us directly at +1 (603) 226 0404 between the hours of 8:30 a.m.– 5:00 p.m. (US Eastern Time) or +44 (0) 1236 373500 between the hours of 8:30 a.m. – 5:00 p.m. (UK GMT).

1.6 Customer Feedback

Thank you for using BittWare products. We appreciate you choosing BittWare for your FPGA development.

If you have a few minutes to spare, we would love to hear from you about your experience with our products or our staff. We know your time is valuable; we would be grateful for any comment at all.

- Please email us at support@bittware.com for any type of feedback
- Or, let us know about a recent Technical Support inquiry at http://koch.link/bwsupportfeedback

2Board Overview

The IA-440i is a low-profile, single-width, PCIe Gen5 x16 card with an Intel Agilex 7 I-Series FPGA. The FPGA is connected to a QSFP-DD port and up to 32GB DDR4. The IA-440i supports both active and passive cooling options.

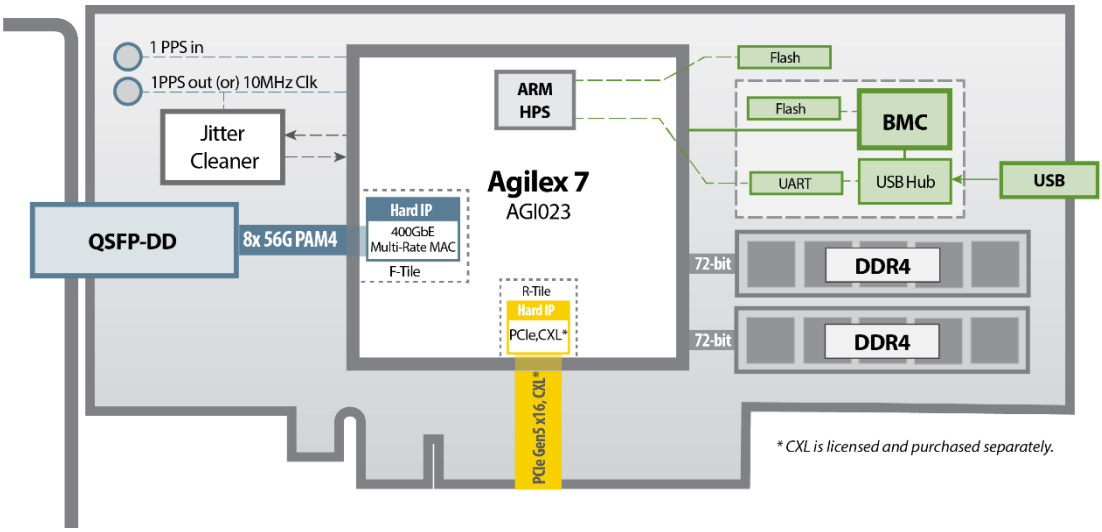
2.1 Key Features

- **Form Factor:** Single width, half height (68.90 mm), low-profile form factor length (167.65mm)
- **FPGA:** Intel Agilex AGI023 FPGA (AGI023: Core speed grade -1: XCVR speed grade –1)
- **Network IOs:** 1 QSFP-DD port supporting 400/200/100/40/10 Gb Ethernet
    - Supports 1x 400GbE, 2x 200GbE, 4x 100GbE, 8x 50GbE
    - Multi-rate hard MAC+FEC for 10/25/100GbE
- **Memory Banks:**
    - 2 banks on-board DDR4 (default 8GB each) x72
- **FPGA Configuration:**
    - Power-on FPGA configuration from flash, dual image
    - USB-Blaster II Interface for FPGA JTAG access
- **Board Management Controller (BMC 3.0):**
    - Voltage, current, temperature monitoring
    - Power sequencing and reset
    - Field upgrades
    - FPGA configuration and control
    - Clock configuration
    - Low bandwidth BMC-FPGA comms with SPI link
    - USB 2.0
    - PLDM support
    - Card-level security (future)
- **USB connectivity:**
    - USB access to BMC, USB-UART
- **User clocks**
- **User LEDs**

2.2 Block Diagram

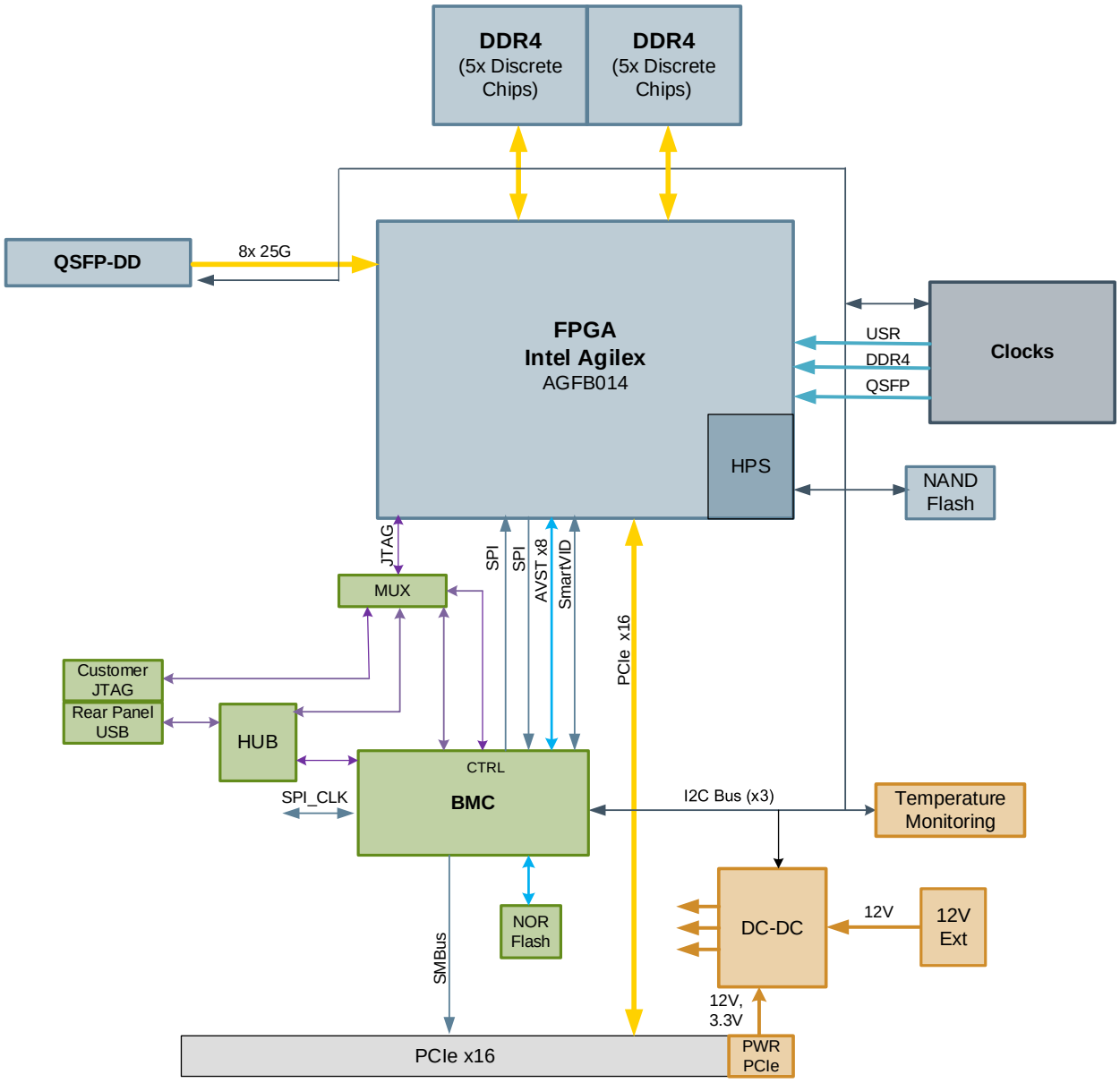
The diagram below shows the key functional features of the IA-440i. The FPGA is used to implement the PCIe Gen5, DDR4, QSFP-DD, and Board Management Controller interfaces while leaving ample room for user applications. The board is also designed to efficiently handle cooling for higher powered FPGA applications while maintaining high throughput.

Figure 1: IA-440i Block Diagram



NOTE: Refer to the images in the Board Layout section for actual component and connector locations.

Figure 2: IA-440i Functional Block Diagram



2.3 Board Layout

This section shows where the main components on the IA-440i are located. Each of these is described in more detail later in this document.

Figure 3: Top View

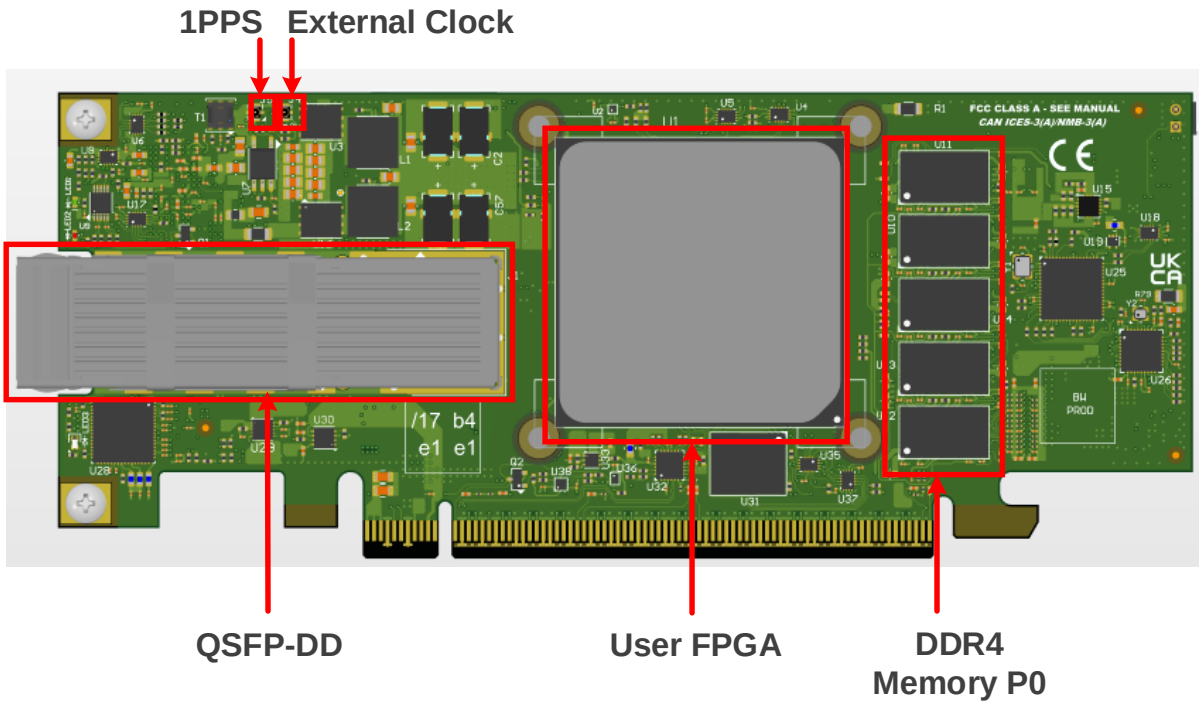
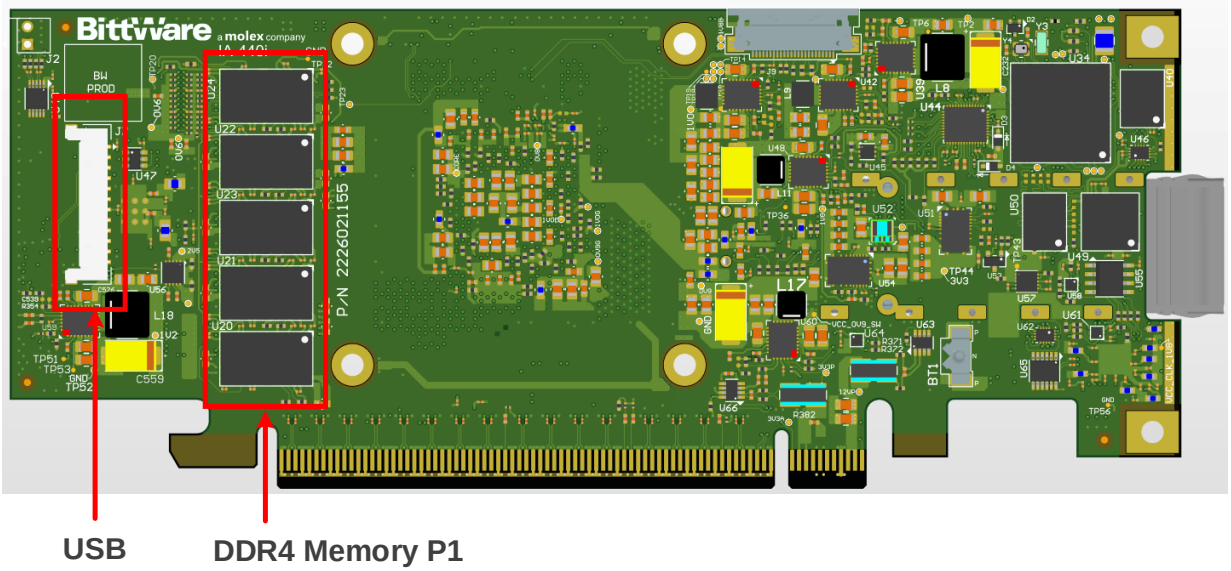


Figure 4: Bottom View



2.4 Key Components

The tables below list the manufacturer and part number of the board's key components and connectors.

Table 3: Component List

Component	Part Number	Manufacturer
Agilex FPGA	FPGA part number is order dependent.	Intel
BMC configuration Flash(x2)	MT25QU02GCBB8E12-0SIT	Micron
HPS NAND flash (not populated)	MT29F4G08ABBDAH4-IT:D	Micron
DDR4	MT40A1G16KNR-075:E	Micron
I2C switch	TCA9548ARGER	Texas Instruments
Microcontroller	MIMXRT1165CVM5A	NXP
MAC ID PROM	AT24C02D-SSHM-T	Microchip Technology
USB controller	CY7C68013A-56LTXI	Cypress Semiconductor
USB hub	USB2534I-1080AENTR	Microchip Technology
USB to UART	FT4232HQ	FTDI
24MHz Crystal (Y1, Y3)	XRCGB24M000F3M00R0	Murata Manufacturing
12MHz Clock (Y2)	ABMM-12.000MHZ-N2-T	Abracon
32.768KHz Crystal (Y4)	FX135A-327	Fox Electronics
Jitter Cleaner	SiT95148	SiTime

Table 4: Connector List

Connector	Part Number	Manufacturer
QSFP-DD (J1)	2027180100	Molex
Ext. clock (J4) 1 PPS (J5)	RECE.20369.001E.01	TAOGLAS
USB JTAG (J7)	5040501291	Molex

2.5 Programmable Devices

The following table describes the programmable non-volatile devices on the IA-440i.

Device	Description	Programming Method(s)	Usage
BMC	Local microcontroller, flash based	BittWare factory-programmed	Stores code and configuration options. Clock configuration stored in local flash. FRU data.
Configuration Flash	FPGA boot configuration	USB or PCIe (via BMC), or pre-programmed	256MB configuration space. Currently supporting single default flash image. Future BMC release will support multiple images and fallback
MAC ID & Serial Number PROM	Contains unique 128-bit serial number	Base MAC ID factory programmed	The FPGA will read the base MAC ID and can use 8 sequential addresses. The serial number can be read and used for software feature licensing. The MAC PROM is programmed at BittWare's factory with card unique information. For more information about the content of the MAC PROM, and how to access its content, see VPD EPROM
SiT95148 clock generator	Jitter cleaner	Written by BMC during power-up sequence	Stored in BMC, user writable with host side utility. Host side utility supported from SDK 2023.2.

Letter of Volatility: Please contact BittWare support if you need a letter of volatility for this board.

2.6 Board Options and Variants

This Hardware Reference Guide describes a default hardware configuration of the IA-440i. Keep in mind that your board may be configured differently.

2.7 Development Tools, Example Designs, and IP

BittWare offers several soft deliverables to help customers develop their FPGA applications:

- **The BittWare Software Development Kit (SDK)** is a cross-platform collection of drivers, libraries, modules, and utilities that aid you in debugging and developing applications using BittWare PCIe cards. The SDK is free for 1 year, then requires a yearly maintenance fee.
- **The BittWare Card Support Package (CSP) for the SDK** contains card specific FPGA Gateware and Software to develop on your FPGA cards. The CSP contains several items specific to your FPGA card:
    - Card Test (previously known as Built-In Self-Test, or BIST)
    - Card documentation
    - BittWare gateware and software example designs
    - Software utilities
- **Intel Quartus Prime Pro licenses** – 1-year node-locked Developer Kit Licenses - Includes OpenCL support. Downloads, documentation, and support are available at Intel.com.
- **Intel FPGA IP cores** – Many FPGA IP blocks are available as part of Intel Quartus Prime Pro; however, some others are add-on purchases. Downloads, documentation, and support are available at Intel.com.

BittWare also works very closely with FPGA IP developers for solutions based on DPDK, NVMe, etc. Contact your BittWare sales representative for more information at https://www.bittware.com/contact/.

2.8 TeraBox Server Integration

When it comes to development, TeraBox servers are delivered pre-integrated with your choice of BittWare FPGA accelerators. The TeraBox servers are pre-configured with your choice of operating system and FPGA development tools. This allows you to develop and deploy quicker with reduced risk and cost.

TeraBox servers are also deployment-ready for mission-critical applications. BittWare can take care of qualification testing as well as branding. TeraBox servers can be configured to include your host-based application as well as pre-loaded FPGA bitstreams executables, which translates to the servers being ready to run as soon as your customer receives them.

BittWare supports a variety of leading server vendors. As part of Molex, we can handle global supply chain and logistics. We can cater to a range of application environments such as data center and at the edge. Lastly, through OEM programs, you have the option of purchasing selected TeraBox servers directly from server vendors such as Dell, HPE, and Lenovo.

For more information, contact your BittWare Sales representative or visit https://www.bittware.com/fpga/servers-systems/.

3Board Setup

3.1 Handling, Unpacking, and Shipping Tips

Warning! The IA-440i contains electro-static discharge (ESD) sensitive devices. Be sure to follow the standard handling procedures for ESD sensitive devices, taking proper precautions to ground yourself and the work area before removing the board from its static shielding bag. If you fail to follow proper handling procedures, you could damage the board.

3.1.1 ESD Handling Tips

Effective ESD control and proper ESD handling will maintain the reliability of your BittWare products. Please follow the guidelines listed below to avoid ESD damage to the IA-440i.

- Transport the board only in ESD shielding bags or shielding containers.
- Do not remove the board from its static shielding bag when outside an EPA (ESD Protected Area).
- Wear a grounding wrist strap when handling the board. BittWare also recommends using foot/heel straps in combination with static dissipative flooring.
- When handling the board, hold it by its edges, being careful not to touch any of its components.
- All work benches should be properly grounded and have a conductive surface to eliminate ESD. Placing the board on top of the static shielding bag does not offer any ESD protection.

NOTE: For more information on development of an ESD Control program, contact BittWare or refer to ANSI/ESD S20.20-2007.

3.1.2 Unpacking the IA-440i

To unpack the card:

1. Observe all precautions described in the ESD Handling Tips above to prevent damage from electro-static discharge (ESD).
2. Carefully remove the card from the shipping box. Save the box and packing materials in case you need to reship the card.
3. Carefully examine the card, checking for damage. If the board is damaged, do not install it. Contact BittWare technical support.

3.1.3 Shipping the IA-440i

Should you need to ship the IA-440i back to BittWare, please pack it in its original packaging to avoid damage during shipping.

If you are shipping the card as part of an integrated server, it is your responsibility to ensure that the bracket, packaging, and shipping materials are adequate to prevent damage during shipment. When BittWare provides systems pre-integrated into a server, we ship the integrated product on a pallet to minimize the chance of damage. We recommend this method for customer shipments of integrated systems as well.

3.1.4 Hot Surface Warning

When the IA-440i is operational, the card generates heat. The heat is dispersed using various heatsinks and the rear stiffening frame. Take care on any IA-440i exposed metal surface as it may be too hot to touch.

3.2 Where to find:

- **Installation Instructions**: To get started with your board, we recommend following the installation procedure in the IA-440i Getting Started Guide. The Getting Started Guide is available on the Developer Site on the product page for the IA-440i.
- **Development Tools**: The BittWare SDK is a suite of development tools that provides the main interface between the IA-440i and the host system. When your maintenance is active, you can download the SDK latest version and view the SDK documentation on the SDK Support Center section of the Developer Site.
- **FPGA Card Test, Examples, and Software Utility**: These items are available in the IA-440i Card Support Package for the BittWare SDK. A variety of examples and reference designs are available for you to use as a starting point. You can download these from the IA-440i product page on the BittWare Developer Site.
- **Card Documentation:** All card documentation is available for download on the IA-440i product page on the BittWare Developer Site.

Note: The latest versions of the Software Developer Kit and the Card Support Package are only available to customers with an active SDK maintenance contract.

3.3 Warranty

This section outlines the handling guidelines that are allowed within the warranty. Always follow the ESD Handling Tips (see ESD Handling Tips). Do not move or replace any component that was installed by BittWare (DIMMs, cables, etc.) without reaching out to BittWare support. The support team will ensure these parts are replaced safely to avoid any possible damage to the card; in many cases an RMA will be required. Moving these components without recommendation from the support team will void the warranty of the card.

Other components that were not preinstalled (QSFPs, cables, etc.) can be moved or replaced.

For any clarification on operations allowed under the warranty, please reach out to BittWare. See Contacting BittWare for instructions on how to contact BittWare Support to ask technical questions.

3.4 RMA – Returning your product to BittWare

Before BittWare issues an RMA, we will attempt to fix any issues remotely. We also capture as much debugging information as possible to help our production team replicate the issue at our factory. This

process ensures a quicker resolution, and in many cases avoids having to return the card back to BittWare.

RMA resolution time varies depending on the issue and the amount of investigation, retest, and rework required. The lead time for replacement parts and the availability of our rework factory also impacts the RMA resolution time. We can estimate the RMA resolution time when we receive the RMA board at our factory.

See Contacting BittWare for instructions on how to contact BittWare Support to request an RMA.

3.5 Card Test

The IA-440i is delivered preprogrammed with a Card Test application that verifies the key features of the product. Refer to the BittWare *IA-440i Getting Started Guide* for instructions on how to run the Card Test application. The Card Test is a useful example of how to use all the features of the IA-440i. The Card Test is available for download on the BittWare Developer Site.

The Card Test design demonstrates how to use all board features and should be used by HDL developers as the main reference and documentation. The Card Test is an example design which instantiates Intel IP blocks as required for the IA-440i hardware. The Card Test contains IP to access the features of the Board Management Controller (BMC), the Intel PCIe Hard IP, etc.

3.6 FPGA Configuration

The IA-440i can automatically load an FPGA design from Flash at power on. There are several ways to program the FPGA:

JTAG Chain using external USB-Blaster or Blaster II – The IA-440i does not incorporate an embedded USB-Blaster II, unlike previous BittWare IA series products. You will need an external Intel USB programming pod to access the FPGA JTAG. Connecting to the board via USB pod allows access to the JTAG chain with Quartus Programmer. Using this method, you can reconfigure the FPGA directly. The JTAG chain also provides debug access to the board and enables the use of various JTAG-based debug utilities such as Intel's Signal Tap Logic Analyzer and Intel's System Console.

User Flash Interface – The on-board 2Gb configuration flash, for FPGA configuration, can be programmed over USB with the FPGA user application image currently. Support is being added to allow programming of the configuration flash via the FPGA design if it includes the **BittWare BMC3 IP** block. Once the user design has reprogrammed the flash, the FPGA will be configured with the updated design at the next power cycle or after you launch a soft reconfigure request.

The Intel Quartus tools cannot be used to program the flash as the FPGA is not directly attached to the flash on the IA-440i. You will need to use the SDK bw_bmc_fpga_load utility to program the Flash.

The current tested method of programming the flash is via USB (by using a .rbf file).

For details on FPGA configuration, refer to the IA-440i FPGA Developer Guide.

4FPGA

4.1 User FPGA Supported Devices

The following is a list of FPGA devices that this card supports:

Table 5: Supported FPGA Devices

Part Number	Description
AGIB023R18A1E2VR0 (engineering silicon)	Intel Agilex AGI023 in a 1805A package Core speed grade 2 XCVR speed grade 1 HPS
AGIB023R18A1E1V (default; production silicon)	Intel Agilex AGI023 in a 1805A package Core speed grade 1 XCVR speed grade 1 HPS

4.2 FPGA Implementation Details

4.2.1 FPGA Bank Usage

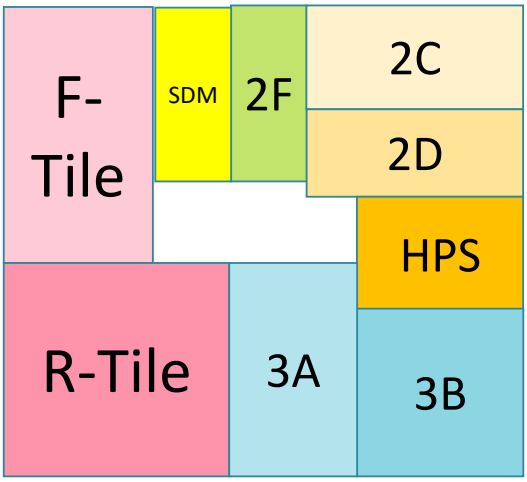
The FPGA banks are powered by the supplies given in Table 6. FPGA core voltage (V_{core}) is 0.81V by default and adjusted automatically to the appropriate VID level by the BMC.

Table 6: FPGA Voltage Settings

Signals	Bank	Bank IO Voltage
PCIe x16	14C	0V9
FPGA Configuration I/O	SDM	1.8V
HPS	HPS	1.8V
LEDS, I^2C & Misc	2F	1.2V
DDR4	2C, 2D, 3A & 3B	1.2V
QSFP	12A	3.3V
MCIO[1]	12A	

[1] MCIO is only on the IA-640i variant.

Figure 5: FPGA Bank Usage



4.2.2 FPGA Hard IP Usage

The IA-440i uses the following IP on the FPGA:

Table 7: FPGA Hard IP

Hard IP	Usage	Tile
Multi-rate hard MAC+FEC for 10/25/100/200/400GbE	1x QSFP-DD channel	F-tile
PCIe	x16 Gen5 interface (CXL support)	R-tile

4.2.3 HPS

The Hard Processor System in the FPGA supports the following:

- Dedicated NAND flash[2]
- UART
- Standard mode
- HPS JTAG accessible via FPGA JTAG

Refer to the FPGA Developer Guide for more detail.

Table 27 HPS Signal Connections

FPGA Pin	Signal Description	FPGA Block
AC3	HPS_CLK	HPS
UART		
AG5	HPS_UART_TXD	HPS

[2] Not populated on Rev 0 hardware.

AN3	HPS_UART_RXD	HPS
Flash		
AH10	HPS_NAND_D0	HPS
AN9	HPS_NAND_D1	HPS
AP8	HPS_NAND_D2	HPS
AL9	HPS_NAND_D3	HPS
AJ9	HPS_NAND_D4	HPS
AM8	HPS_NAND_D5	HPS
AH8	HPS_NAND_D6	HPS
AL7	HPS_NAND_D7	HPS
AJ11	HPS_NAND_WE_L	HPS
AP10	HPS_NAND_RE_L	HPS
AL11	HPS_NAND_WP_L	HPS
AN7	HPS_NAND_CLE	HPS
AG9	HPS_NAND_ALE	HPS
AP6	HPS_NAND_RB_L	HPS
AF8	HPS_NAND_CE_L	HPS

5PCIe Interface

5.1 Mechanical Details

5.1.1 PCIe Card Form Factor

The IA-440i is a half-height, half-length (low-profile), single-width PCIe add-in card with a 16-lane electrical and 16-lane mechanical interface. The PCIe interface complies with the PCIe 5.0 specification.

5.1.2 PCIe Host Interface

The IA-440i card has a 16-lane mechanical and electrical PCIe 5.0 interface. The IA-440i does not feature a dedicated PCIe device for PCIe host transfers; the user FPGA design must include the Intel PCIe Hard IP core.

Intel supports multiple configurations of the PCIe core as part of QSYS. Users can set up the Intel IP core for anything from 1 lane at PCIe 1.0 to 16 lanes at PCIe 5.0.

The PCIe interface capabilities and features are:

- Host PCIe bandwidth up to 64 GB/s[3] (16 lanes at 32Gbps – PCIe 5.0)

5.1.3 PCIe Endpoint Characteristics

The card is preprogrammed with the Card Test when shipped from the BittWare factory. When connected to a PCIe host, the card will enumerate on the PCIe bus with the following details:

- PCI Vendor ID: 0x12BA
- PCI Device ID: 0x0073

The PCIe end-points properties are accessible with the `lspci` command on Linux or using the Windows Hardware Manager.

5.2 Interface Description

5.2.1 PCIe Enumeration

The PCIe specification requires that a PCIe endpoint be ready for PCIe enumeration within 100ms of the host system powering on. Agilex by default uses an autonomous HIP mode which brings up PCIe before the rest of the FPGA is configured. For FPGA cards, it means that the FPGA should be configured and out of reset within 100ms of power on. However, this requirement is more often widened by host servers and workstations effectively allowing the FPGA more time to complete its configuration.

[3] Maximum theoretical data rate for 16 lanes of PCIe 5.0; the actual host bandwidth depends on the host hardware (motherboard, chipset, processor, etc.), the PCIe IP settings, and the FPGA design itself.

5.2.2 SMBus Features

The SMBus signals are connected to the BMC, reserved for future use.

5.2.3 PCIe Reset Requirements

Since the IA-440i is a PCIe card, it is a slave to a host processor that is the root complex of the PCIe bus. Therefore, the reset for this board comes through the PCIe bus from the host.

The mechanism that supports a reliable initialization of the firmware and software running on the IA-440i is as follows:

1. The board powers up and supplies are sequenced by the BMC, after which the board comes out of reset.
2. When the power supplies are stable, the BMC LED (D5) blinks green, the configuration logic is released, and the FPGA configuration starts.
3. The BMC then programs the clock chip.
4. After FPGA configuration, PCIe training and reset should occur.
5. The release of the PCIe reset by the host also deactivates the global reset to the internal FPGA design.
6. After PCIe enumeration, a soft reset comes from the PCIe core to the rest of the internal FPGA logic to start the firmware.

5.2.4 PCIe Pinout

Table 8 shows the FPGA pins used for the PCIe interface

Table 8: FPGA Pins used for Host PCIe (x16) Interface

FPGA Pin	Signal Description	Tile
AL47	PCIe Host Lane 0 RX (P)	Bank 14C
AM46	PCIe Host Lane 0 RX (N)	Bank 14C
AG47	PCIe Host Lane 1 RX (P)	Bank 14C
AH46	PCIe Host Lane 1 RX (N)	Bank 14C
AC47	PCIe Host Lane 2 RX (P)	Bank 14C
AD46	PCIe Host Lane 2 RX (N)	Bank 14C
W47	PCIe Host Lane 3 RX (P)	Bank 14C
Y46	PCIe Host Lane 3 RX (N)	Bank 14C
R47	PCIe Host Lane 4 RX (P)	Bank 14C
T46	PCIe Host Lane 4 RX (N)	Bank 14C
L47	PCIe Host Lane 5 RX (P)	Bank 14C
M46	PCIe Host Lane 5 RX (N)	Bank 14C
G47	PCIe Host Lane 6 RX (P)	Bank 14C
H46	PCIe Host Lane 6 RX (N)	Bank 14C
K44	PCIe Host Lane 7 RX (P)	Bank 14C
J43	PCIe Host Lane 7 RX (N)	Bank 14C
D46	PCIe Host Lane 8 RX (P)	Bank 14C
C45	PCIe Host Lane 8 RX (N)	Bank 14C

F44	PCIe Host Lane 9 RX (P)	Bank 14C
E43	PCIe Host Lane 9 RX (N)	Bank 14C
G41	PCIe Host Lane 10 RX (P)	Bank 14C
H40	PCIe Host Lane 10 RX (N)	Bank 14C
C41	PCIe Host Lane 11 RX (P)	Bank 14C
D40	PCIe Host Lane 11 RX (N)	Bank 14C
B38	PCIe Host Lane 12 RX (P)	Bank 14C
A37	PCIe Host Lane 12 RX (N)	Bank 14C
F38	PCIe Host Lane 13 RX (P)	Bank 14C
E37	PCIe Host Lane 13 RX (N)	Bank 14C
C35	PCIe Host Lane 14 RX (P)	Bank 14C
D34	PCIe Host Lane 14 RX (N)	Bank 14C
G35	PCIe Host Lane 15 RX (N)	Bank 14C
H34	PCIe Host Lane 15 RX (P)	Bank 14C
AR41	PCIe Host Lane 0 TX (P)	Bank 14C
AT40	PCIe Host Lane 0 TX (N)	Bank 14C
AP44	PCIe Host Lane 1 TX (P)	Bank 14C
AN43	PCIe Host Lane 1 TX (N)	Bank 14C
AL41	PCIe Host Lane 2 TX (P)	Bank 14C
AM40	PCIe Host Lane 2 TX (N)	Bank 14C
AK44	PCIe Host Lane 3 TX (P)	Bank 14C
AJ43	PCIe Host Lane 3 TX (N)	Bank 14C
AG41	PCIe Host Lane 4 TX (P)	Bank 14C
AH40	PCIe Host Lane 4 TX (N)	Bank 14C
AF44	PCIe Host Lane 5 TX (P)	Bank 14C
AE43	PCIe Host Lane 5 TX (N)	Bank 14C
AC41	PCIe Host Lane 6 TX (P)	Bank 14C
AD40	PCIe Host Lane 6 TX (N)	Bank 14C
AB44	PCIe Host Lane 7 TX (P)	Bank 14C
AA43	PCIe Host Lane 7 TX (N)	Bank 14C
W41	PCIe Host Lane 8 TX (P)	Bank 14C
Y40	PCIe Host Lane 8 TX (N)	Bank 14C
V44	PCIe Host Lane 9 TX (P)	Bank 14C
U43	PCIe Host Lane 9 TX (N)	Bank 14C
R41	PCIe Host Lane 10 TX (P)	Bank 14C
T40	PCIe Host Lane 10 TX (N)	Bank 14C
P44	PCIe Host Lane 11 TX (P)	Bank 14C
N43	PCIe Host Lane 11 TX (N)	Bank 14C
L41	PCIe Host Lane 12 TX (P)	Bank 14C
M40	PCIe Host Lane 12 TX (N)	Bank 14C

V38	PCIe Host Lane 13 TX (P)	Bank 14C
U37	PCIe Host Lane 13 TX (N)	Bank 14C
P38	PCIe Host Lane 14 TX (P)	Bank 14C
N37	PCIe Host Lane 14 TX (N)	Bank 14C
K38	PCIe Host Lane 15 TX (N)	Bank 14C
J37	PCIe Host Lane 15 TX (P)	Bank 14C

6 External Interfaces

6.1 Overview

Table 9: External Interface Summary

Feature	Ref Des	Width	Max Rating	Spec(s)
PCIe	P1	x16	Gen5 (32Gbps)	PCI Express Base Specification Revision 5.0, Version 1.0
QSFP-DD	J1	x8	28G NRZ or 56G PAM4	
1PPS	J5	x1	1 Hz	LVTTL (2.5V to 3.3V) Pulse per Second
RefClk	J4	x1	10MHz	200mV to 3V3 pk-pk
USB	J7	x1	480Mbps	USB 2.0

6.2 QSFP-DD

The IA-440i features one QSFP-DD port. The QSFP-DD high speed interface is directly driven from IP within the user FPGA design. Intel provides IP cores for multiple high-speed protocols compatible with the IA-440i which all have their own reference clock requirements. The IA-440i is populated with an on-board frequency clock device which, by default, feeds a 156.25 MHz clock (for 100/40/10 GbE) to the dedicated transceiver IP reference clock FPGA pins.

6.2.1 Supported Speeds

A range of protocols can be implemented using Intel's IP core QSYS library. For such IP cores, different reference clock frequencies might be required. The QSYS IP Library contains several pre-set files and automated rule checks which enable the IA-440i user to quickly target the FPGA with multiple network protocols.

BittWare allocates 8 dedicated MAC addresses per IA-440i. These addresses are programmed in the ID PROM.

The BMC controls access the QSFP-DDs control/status signals.

Table 10: Transceiver speed and MAC Core availability

QSFP-DD Port Number	Data Rate	MAC Core Availability*
QSFP-DD 0	58 Gbps/lane (400/200/100/25/10 GbE)	400 GbE Hard IP multi-rate MAC core (F-tile)

6.2.2 QSFP-DD Clocking

The FTILE clocks connect to the F-tile global clock network.

Table 11 F-Tile Clock Connections

FPGA Pin	Clock Signal	FPGA Bank
CB38	FTILE_REFCLK_CH3_P	Bank 12A

CA37	FTILE_REFCLK_CH3_N	Bank 12A
BT38	FTILE_REFCLK_CH4_P	Bank 12A
BU37	FTILE_REFCLK_CH4_N	Bank 12A
BN37	FTILE_REFCLK_CH5_P	Bank 12A
BR37	FTILE_REFCLK_CH5_N	Bank 12A

6.2.3 FPGA to QSFP Pin Mapping

The eight SerDes bidirectional lanes are connected to a single FPGA transceiver quad (12A). It is designed for up to 58Gbps PAM4. The traces are designed to meet the OIF CEI-28G-VSR specification requirements.

The Intel QSF constraints file is the point of reference for pin mappings; however, *Table 12 QSFP-DD Pinout Table* illustrates how the QSFP-DD spec pin naming correlates to the design naming.

Table 12 QSFP-DD Pinout Table

Signal	Direction to FPGA	FPGA Pin	QSFP pin
QSFP_CLK_P	Input		N/A
QSFP_CLK_N	Input		N/A
QSFP0_RX_P0	Input	AR47	17
QSFP0_RX_N0	Input	AT46	18
QSFP0_RX_P1	Input	AV44	22
QSFP0_RX_N1	Input	AU43	21
QSFP0_RX_P2	Input	AW47	14
QSFP0_RX_N2	Input	AY46	15
QSFP0_RX_P3	Input	BB44	25
QSFP0_RX_N3	Input	BA43	24
QSFP0_RX_P4	Input	BC47	36
QSFP0_RX_N4	Input	BD46	37
QSFP0_RX_P5	Input	BG47	3
QSFP0_RX_N5	Input	BH46	2
QSFP0_RX_P6	Input	BL47	33
QSFP0_RX_N6	Input	BM46	34
QSFP0_RX_P7	Input	BR47	6
QSFP0_RX_N7	Input	BT46	5
QSFP0_TX_P0	Output	AW41	55
QSFP0_TX_N0	Output	AY40	56
QSFP0_TX_P1	Output	BC41	60
QSFP0_TX_N1	Output	BD40	59
QSFP0_TX_P2	Output	BF44	52
QSFP0_TX_N2	Output	BE43	53
QSFP0_TX_P3	Output	BG41	63
QSFP0_TX_N3	Output	BH40	62
QSFP0_TX_P4	Output	BK44	74
QSFP0_TX_N4	Output	BJ43	75
QSFP0_TX_P5	Output	BL41	41
QSFP0_TX_N5	Output	BM40	40

QSFP0_TX_P6	Output	BP44	71
QSFP0_TX_N6	Output	BN43	72
QSFP0_TX_P7	Output	BR41	44
QSFP0_TX_N7	Output	BT40	43

6.2.4 QSFP-DD Control Signals

QSFP-DD control signals are connected to the BMC. These signals can be managed one of two ways:

- Via I2C reads and writes from the BMC
- Via virtual pins implemented by the BittWare Card Management IP Block – *See the IA-780i FPGA Developer's Reference Guide for more information*

QSFP-DD Control Signals

Signal Name	Description	Direction to Module	Connected to
I2C_QSFP_SCL	I2C Clock	Input	BMC Pin – D11 (GPIO_DISP_B1_02)
I2C_QSFP_SDA	I2C Data	Bidirectional	BMC Pin – E11 (GPIO_DISP_B1_03)
QSFP_PRESNT_L	Module installed	Output	BMC Pin – M10 (GPIO_SNVS_03)
QSFP_INT_L	Interrupt	Output	BMC Pin – L9 (GPIO_SNVS_02)
QSFP_LP	Low Power Mode	Input	BMC Pin – P10 (GPIO_SNVS_01)
QSFP_RST_L	Reset	Input	BMC Pin – N10 (GPIO_SNVS_04)

6.2.5 Cage and Connector

A double density cage permits up to 8 high-speed links to external devices. This format allows both standard x4 modules and cables in addition to the octal versions. This connector is the same width as a standard cage but adds two more rows which makes it deeper than the quad cage.

- The cage is a Press Fit Molex 2031431355
- The connector is a Molex 202718-0100

6.2.6 Validated Cables and Transceiver Settings

A list of validated cables will be available soon.

7 Memory

7.1 DDR4

The IA-440i has two on-board/discrete banks of DDR4. The banks are 72 bits (64 bits + 8-bit ECC) wide and configured as 8GB capacity standard operating at 3200 MT/s. The table below shows the supported memory speeds on the card.

FPGA	Bank Size (Bytes)	Bank Speed (MTPS)
Engineering silicon	8G	2666
Production silicon	8G	3200
Production silicon	16G	2666

Note: The interface runs at DDR4-3200 for -1 speed grade FPGAs and at DDR4-2666 for -2 speed grade FPGAs.

7.1.1 DDR4 QSYS Parameter Files

QSYS parameter files (QPRS) for the DDR4 banks can be generated from the BittWare Card Test memory IP files. Instantiate the “Agilex External Memory Interfaces” (or EMIF) within the FPGA design and use the parameters from these QPRS files.

7.1.2 Clocking the DDR4 Bank

The Intel DDR4 SDRAM IP is supplied with 33.3333MHz reference clocks as detailed in Table 13: DDR4 Reference Clocks.

Table 13: DDR4 Reference Clocks

Source	FPGA Pin	FPGA Signal Name	I/O Standard
SiT95148	CL7	p0_ddr4_clk_p[0]	LVDS18
SiT95148	CK8	p0_ddr4_clk_n[0]	LVDS18
SiT95148	L7	p1_ddr4_clk_p[0]	LVDS18
SiT95148	M8	p1_ddr4_clk_n[0]	LVDS18

7.2 Flash

The 2Gb Flash is used for storing FPGA configuration images. Multiple images can be stored into this flash, dependent upon design size and compression. In a future BMC release this will include a fallback, user and factory image scheme. There are two ways in which the flash can be programmed: via USB or PCI . Refer to the IA-440i Getting Started Guide and the SDK documentation for more detail on programming options. Note that in the current release, the USB path is the supported mechanism. For instructions on generating a .rbf file, refer to the FPGA Developer Guide. The Intel Quartus tool are not a supported method of programming the flash on the IA-440i..

8Clocking

8.1 Clock Circuitry

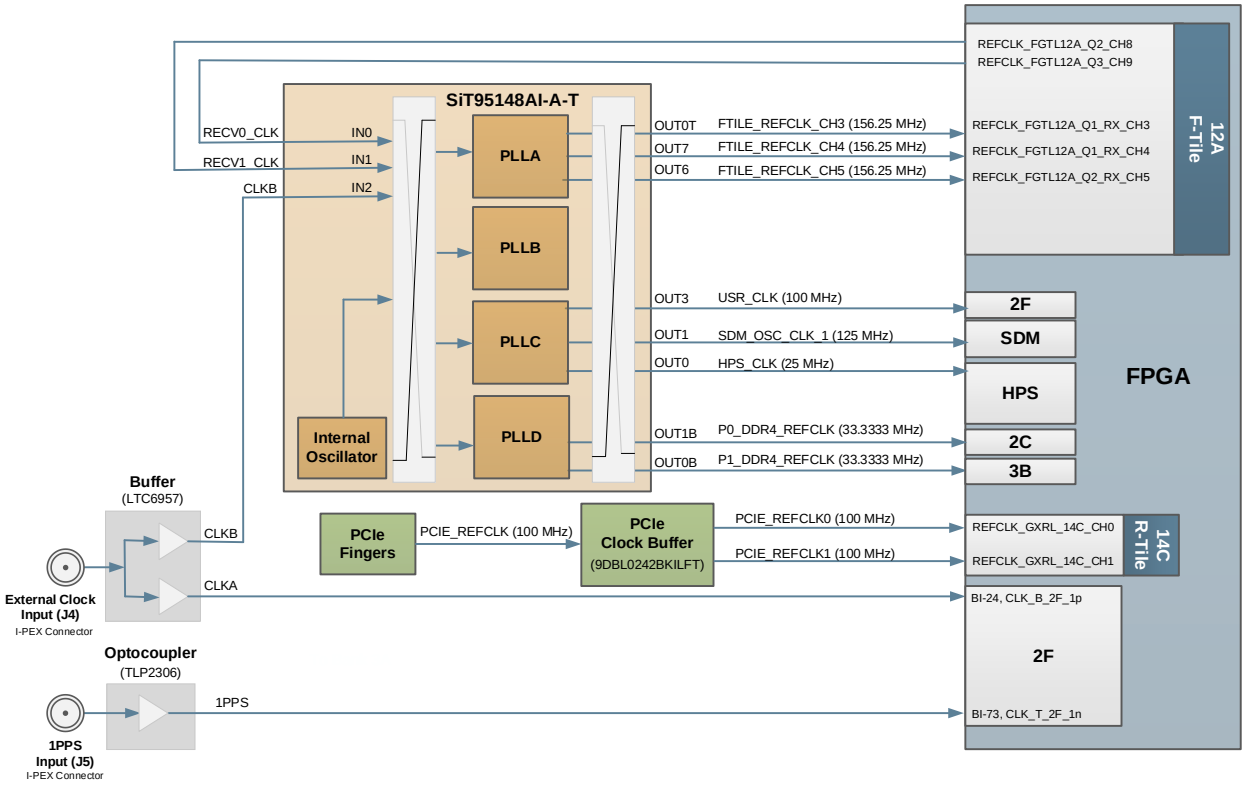
The clocking circuit on this board provides flexible and quality clock sources to the FPGA and associated circuitry without adding significant cost.

Figure 6: Clock Circuitry illustrates the clock design.

The following clocks sources are available to the FPGA design:

- PCIe Clocks
- User Clock
- Configuration Clock
- Memory and General FPGA Clocks
- Network Clock
- HPS Clock
- 1PPS External Synchronization Input
- External Clock Input

Figure 6: Clock Circuitry



8.2 Programmable Clock

The SiTime 95148 is a high performance 11 output MEMs jitter cleaner and clock synthesizer used to generate the User, DDR4 and network clocks. The SiT94148 integrates a high accuracy MEMS resonator which eliminates the need for an external quartz device.

The Sit95148 is programmed by the BMC via its SPI interface on power up to the settings described in this section. The device can also be reprogrammed by the user. The Card Support Package design demonstrates how to program the SiT95148 using a configuration file generated through the SiTime TimeMaster utility

8.3 Clock Sources

Table 14: Clock Functions and Frequencies

Source	Schematic Name	Frequency	I/O Standard	Function
SiT95148	FTILE_REFCLK_CH3	156.25MHz	LVPECL25	F-Tile Reference Clock
SiT95148	FTILE_REFCLK_CH4	156.25MHz	LVPECL25	F-Tile Reference Clock
SiT95148	FTILE_REFCLK_CH5	156.25MHz	LVPECL25	F-Tile Reference Clock
SiT95148	PCIE_REFCLK_FTILE	100MHz	HCSL	F-Tile PCIe Clock
SiT95148	PCIE_REFCLK_OC	100MHz	HCSL	MCIO PCIe Clock
SiT95148	USR_CLK	100MHz	LVDS18	User Clock
SiT95148	SDM_OSC_CLK_1	125MHz	LVCMOS18	SDM Clock
SiT95148	HPS_CLK	25MHz	LVCMOS18	HPS Clocks
SiT95148	P0_DDR4_REFCLK	33.3333MHz	LVDS18	P0 DDR Reference Clock
SiT95148	P1_DDR4_REFCLK	33.3333MHz	LVDS18	P1 DDR Reference Clock
9DBL	PCIE_REFCLK0	100MHz	LP-HCSL	PCIe Reference Clock
9DBL	PCIE_REFCLK1	100MHz	LP-HCSL	PCIe Reference Clock
FPGA	RECV0_CLK	N/A	DIFF_SSTL12	Recovered Clock
FPGA	RECV1_CLK	N/A	DIFF_SSTL12	Recovered Clock
FPGA	P0_DDR4_CLK	1600MHz	DIFF_SSTL12	DDR4 Memory Clock
FPGA	P1_DDR4_CLK	1600MHz	DIFF_SSTL12	DDR4 Memory Clock
External	CLKA	10MHz	LVCMOS12	10MHz Reference
External	U1PPS	1Hz	LVCMOS12	1PPS

Table 15 FPGA Clock Pin Locations

FPGA Pin	Signal Description	FPGA Bank
CB38	FTILE_REFCLK_CH3_P	12A
CA37	FTILE_REFCLK_CH3_N	12A
BT38	FTILE_REFCLK_CH4_P	12A
BU37	FTILE_REFCLK_CH4_N	12A
BN37	FTILE_REFCLK_CH5_P	12A
BR37	FTILE_REFCLK_CH5_N	12A
CU19	USR_CLK_P	2F
CV20	USR_CLK_N	2F
BB38	RECV0_CLK_P	12A
BA37	RECV0_CLK_N	12A
BM38	RECV1_CLK_P	12A
BL37	RECV1_CLK_N	12A
CL7	P0_DDR4_REFCLK_P	2C
CK8	P0_DDR4_REFCLK_N	2C
CG13	P0_DDR4_CLK_P	2C
CH14	P0_DDR4_CLK_N	2C
L7	P1_DDR4_REFCLK_P	3B
M8	P1_DDR4_REFCLK_N	3B
L13	P1_DDR_CLK_P	3B
M14	P1_DDR_CLK_N	3B
CC23	CLKA	2F
CT24	U1PPS	2F
AH10	HPS_CLK	HPS
CN33	SDM_OSC_CLK_1	SDM
AR37	PCIE_REFCLK0_P	14C
AT38	PCIE_REFCLK0_N	14C
AG37	PCIE_REFCLK1_P	14C
AH38	PCIE_REFCLK1_N	14C

8.3.1 PCIe Clock

The PCIe clock is brought to the card via the PCIe finger. The clock is fixed at 100MHz and is provided by the host motherboard. This clock is then buffered through a 2:2 buffer (9DBL0242BKILFT) used throughout the IA-780i for any PCIe bus interfaces.

The Intel PCIe IP must use these reference clocks. Each output uses the 1.8V HCSL I/O standard.

See the PCIe standard specification for more information.

8.3.2 User Clock

An on-board clocking circuit feeds a 100MHz LVDS DC coupled clock signal to the FPGA. This clock is for general clocking of the fabric.

It is not recommended that this clock is changed from its default frequency; however, if this is required contact BittWare for details.

8.3.3 DDR4 Clock

The Intel DDR4 SDRAM IP is supplied with 33.3333MHz reference clocks sourced from the SiT95148 synthesizer. (See also **Error! Reference source not found.**).

8.3.4 HPS Clock

The 25MHz clock for the Hard Processor System in the FPGA is sourced from the SiT95148 synthesizer.

8.3.5 Network Clock

The QSFP-DD modules are driven from dedicated FPGA transceivers. These transceivers require a dedicated reference clock pin to use the cleanest clock source and support high I/O standards with tight jitter tolerances.

The SiT95148 can be configured to generate its outputs (the transceiver reference clocks for the QSFP-DDs) from a combination of its inputs;either on-chip MEMS or a recovered clock from the FPGA. The SiT95148 can be configured so the MEMS is the sole input to the PLLs within the clock chip.

Network Power-on Clock (From SiT95148)

The QSFP-DD bank is fed by one of the SiT95148's LVDS coupled clock output signals. The SiT95148 outputs 156.25 MHz by default at power-on.

Network Recovered Clock

The QSFP-DD bank is fed by one of the SiT95148's LVDS output clocks. The SiT95148 can be used to recover the network clock from the QSFP-DD. In this scenario the FPGA F-Tile outputs a recovered clock which is fed into the SiT95148 input. This is then routed through the clock chip to the FPGA.'s QSFP-clock input

8.4 Timestamp and Synchronization

The IA-440i includes 1PPS and 10MHz reference clock inputs, which are IPEX MHF3 connectors toward the front of the board.

8.4.1 1 PPS Input

The 1PPS signal can be used to provide a means of synchronizing the FPGA timing to an external timing signal. It is an optocoupled input and supports levels of 5.5V. It uses an IPEX MHF3 connector on the PCB that can be wired to a connector directly accessible from the PCIe faceplate (as a board configuration option).

FPGA signal name: U1PPS

8.4.2 External Clock Input

The 10 MHz external clock input can be used to synchronize the FPGA timing to an external timing signal. The clock input can be a sine wave that is 1.41Vpp down to 100mVpp into a 50Ω load or up to 5V. It uses an IPEX MHF3 connector on the PCB that can be wired to a connector directly accessible from the PCIe faceplate (as a board configuration option).

The external clock is buffered and is connected to an input of the SiT95148 jitter cleaner and clock generator as well as to the FPGA fabric.

FPGA signal name: CLKA

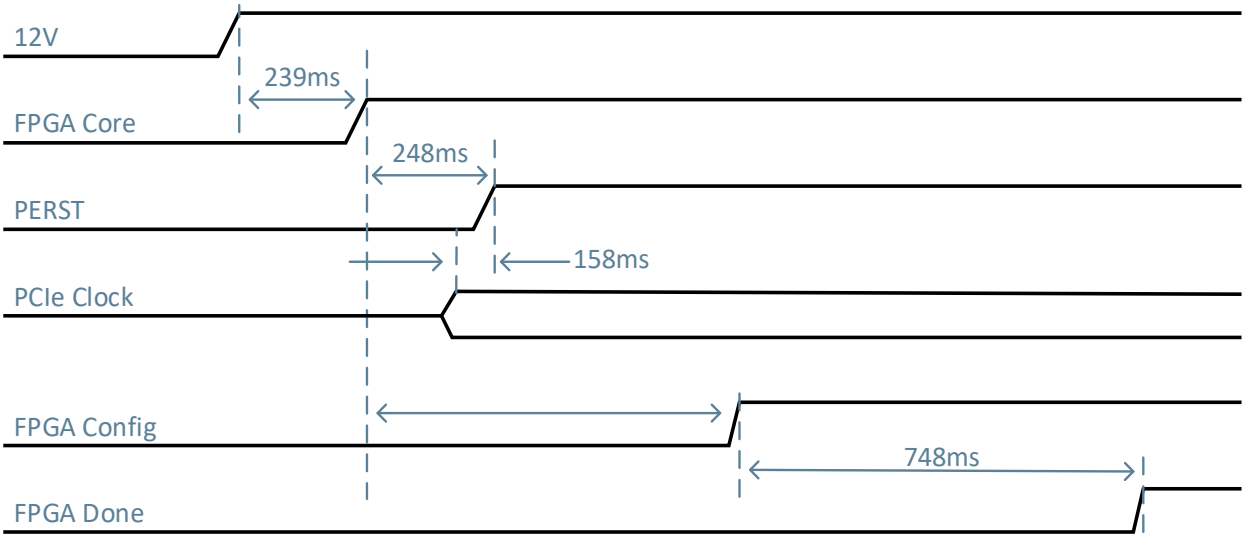
8.5 Start Up Sequence

The IA-440i operates on the PCIe bus. TPVPERL is defined in PCIe CEM to be a minimum of 100ms from 3.3V/12 volts being stable to when PERST# is de-asserted. Note this is a minimum time as defined in the specification. The IA-440i configuration is based on the use of its AVSTx8 interface,

The Agilex series FPGA configuration bitstreams includes PCIe default to activating the PCI HIP Autonomous mode. This mode means that in the period between the initial FPGA section of the bitstream and the completion of the bitstream load when the device enters user mode, the PCIe HIP will return retry requests for configuration TLPs. This extends the PCIe enumeration window timing.

The IA-440i startup timing is shown in Figure 7. The following clock files used to program the clock chip are available on the developer site. For more information, refer to the BMC Reference Guide.

Figure 7 IA-440i Start Up Timing



9Card Management

9.1 BMC

The IA-440i features an advanced system monitoring subsystem, like those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC 3.0), which accepts PLDM commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and PLDM messaging. Access to the BMC is via PCIe or USB. The BittWare SDK also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board. Refer to the BMC Reference Guide for more detail.

The IA-440i is the first BittWare product that makes use of the next generation BittWare BMC architecture. This is an enhanced BMC implementation compared to previous generation BittWare products but initial features and capabilities are similar in form for customers. Future features will add capabilities such as security and the ability to stream FPGA configuration via the USB as examples.

9.1.1 Features and Block Diagram

The BMC subsystem is used to control:

- Power and reset sequencing
- Board support peripherals (such as programmable clock synthesizers)
- MCTP/PLDM support

From an environmental perspective, the BMC provides via PLDM:

- Power supply monitoring
- Current monitoring
- Power supply failure logging (volatile and error persistence logging)
- Power consumption and temperature monitoring (FPGA, QSFP28/QSFPDD modules temperatures)
- Over temperature trip protection (FPGA blanks) and logging (volatile and error persistence logging)

This environmental information is accessed via the software board monitor utility which runs over the USB connection.

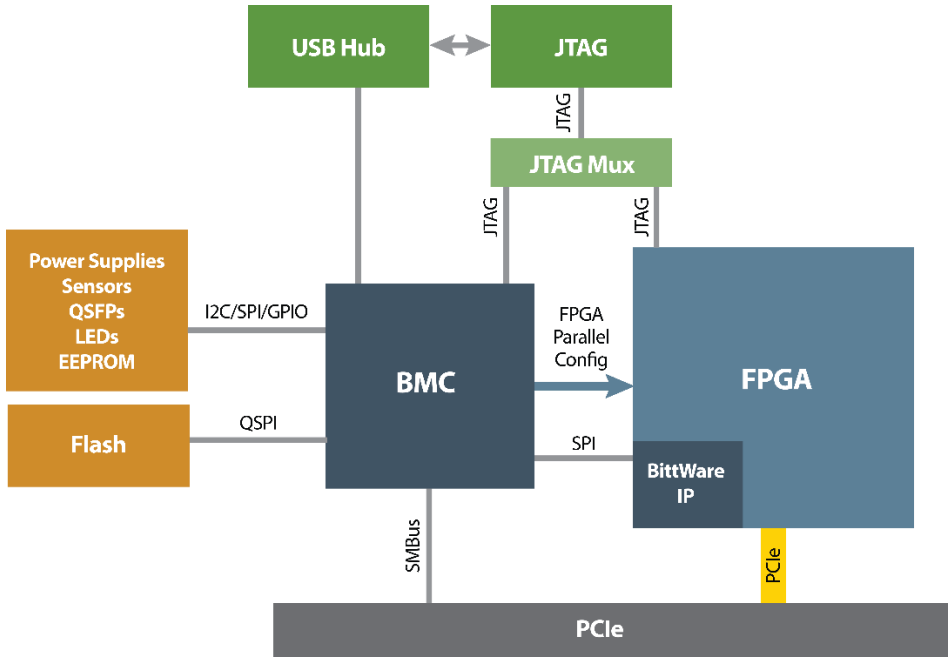
The BMC monitors the FPGA and the board temperature along with voltage, current, and power. The BMC has access to several on-board sensors and implements a shutdown if levels are too high. For a complete list of these sensors and their shutdown values, refer to the *BMC Reference Guide for IA-440i*.

The BMC also provides card-level security features[4]:

- BMC Root of Trust
- BMC and FPGA secure boot
- BMC and FPGA secure upgrade
- Key management

[4] Security capabilities will be added in future soft updates of the BMC 3.0.

Figure 8 BMC 3.0 Block Diagram



9.1.2 BMC Security Features

The BMC 3.0 on the IA-440i includes card-level security features such as key management and signed firmware images. Security is customer-configurable, which allows you to implement the level of security you need for your application. **Security capabilities will be added in future soft updates of the BMC 3.0.**

The BMC functions as a Root of Trust and can be extended to provide security features around the FPGA and flash. The FPGA bitstream storage in the flash is behind the BMC, accessible via BittWare SDK utilities. All I2C peripherals are accessible only through the BMC instead of directly from the FPGA to the I2C bus. The BMC can also be configured to disable external JTAG access.

9.1.3 BMC Utilities

The SDK contains a library for communicating with the BMC via any available data path, including USB or BMC-over-PCIe. Refer to the *BittWare SDK User's Guide* for a list of features and description of the library functions.

The SDK has the following utilities for working with the BMC:

- **bw_bmc_upgrade**: View BMC information, update firmware, reboot the BMC
- **bw_card_monitor**: monitor sensors on the card
- **bw_bmc_configure**: various capabilities, including configure the FPGA, view errors, reboot the BMC
- **bw_bmc_clock_programmer**: read and write clock programs, reprogram clocks
- **bw_bmc_file_ultility**: file access for BMC 3.0
- **bw_bmc_fpga_load**: access configuration flash, view fpga tables
- **bw_bmc_get_logs**: access BMC 3.0 logs

9.1.4 Handling Unused FPGA Pins

Access to the BMC and its associated peripheral devices is possible from the FPGA design. If a user FPGA design does not connect to the BMC, the design must disable access to the FPGA-to-BMC interface by pulling the following pins high:

Pin Name	Location
BMC_IF_PRESENT_N	CH24

The default Quartus settings for unused pins are to tri-state with a weak-pull up. There is no requirement to drive any of the other unused pins to a specific level if the pins listed above are correctly driven.

9.1.5 FPGA Access to the BMC

You can access the BMC via USB and from within your FPGA IP.

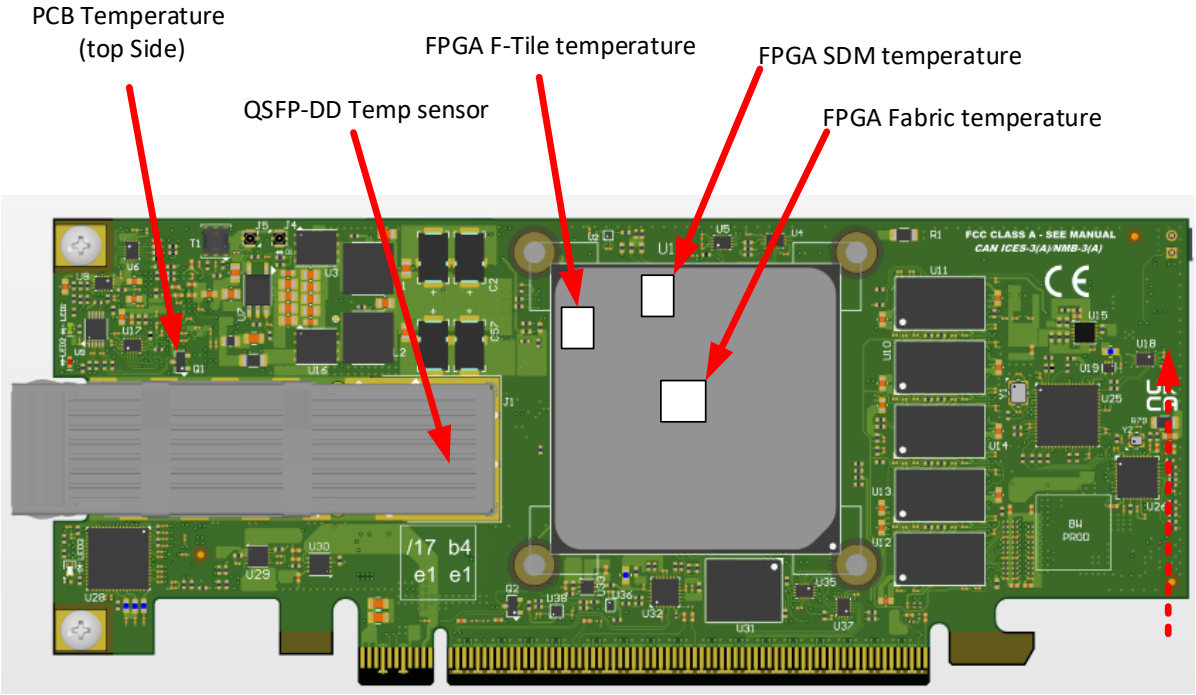
For USB access to the BMC, a rear panel USB C connector is provided for general monitoring and control. The USB interface provides JTAG access to the FPGA and flash via a USB-Blaster-II (driver installed as part of the Quartus installation). An FPGA-driven UART is also provided. See the USB-to-UART section (driver available on the FTDI website).

For FPGA IP access to the BMC, refer to the *FPGA Developer Reference Guide*.

9.2 Thermal Sensors

The card contains several thermal sensors for monitoring FPGA and board temperatures.

Figure 9: IA-440i Temperature Sensor Locations



9.3 I2C Devices

The BMC's hardware I²C ports is directly connected to multiple devices using several dedicated I2C lines. All local devices and the QSFP-DD support 100 kHz operation.

9.3.1 PCIe I2C

An I2C port is routed to the PCIe fingers from the BMC. This interface is used for system-level monitoring and control through such protocol as PLDM and IPMI. It is an isolated interface since in some systems, the signals may be active.

9.3.2 QSFP I2C

An I2C port is routed to the QSFP-DD from the BMC. This interface is used for communicating to the QSFP for monitoring and control.

9.3.3 Power Supply I2C

An I2C port is routed to the power supply and the monitoring circuits from the BMC. This interface is used for system level monitoring and control through protocols such as PLDM.

9.3.4 Clock I2C

An I2C port is routed to the two clock chips from the BMC. This interface is used for system level monitoring to ensure clocks are at the correct frequencies.

Figure 10: I²C Device Diagram

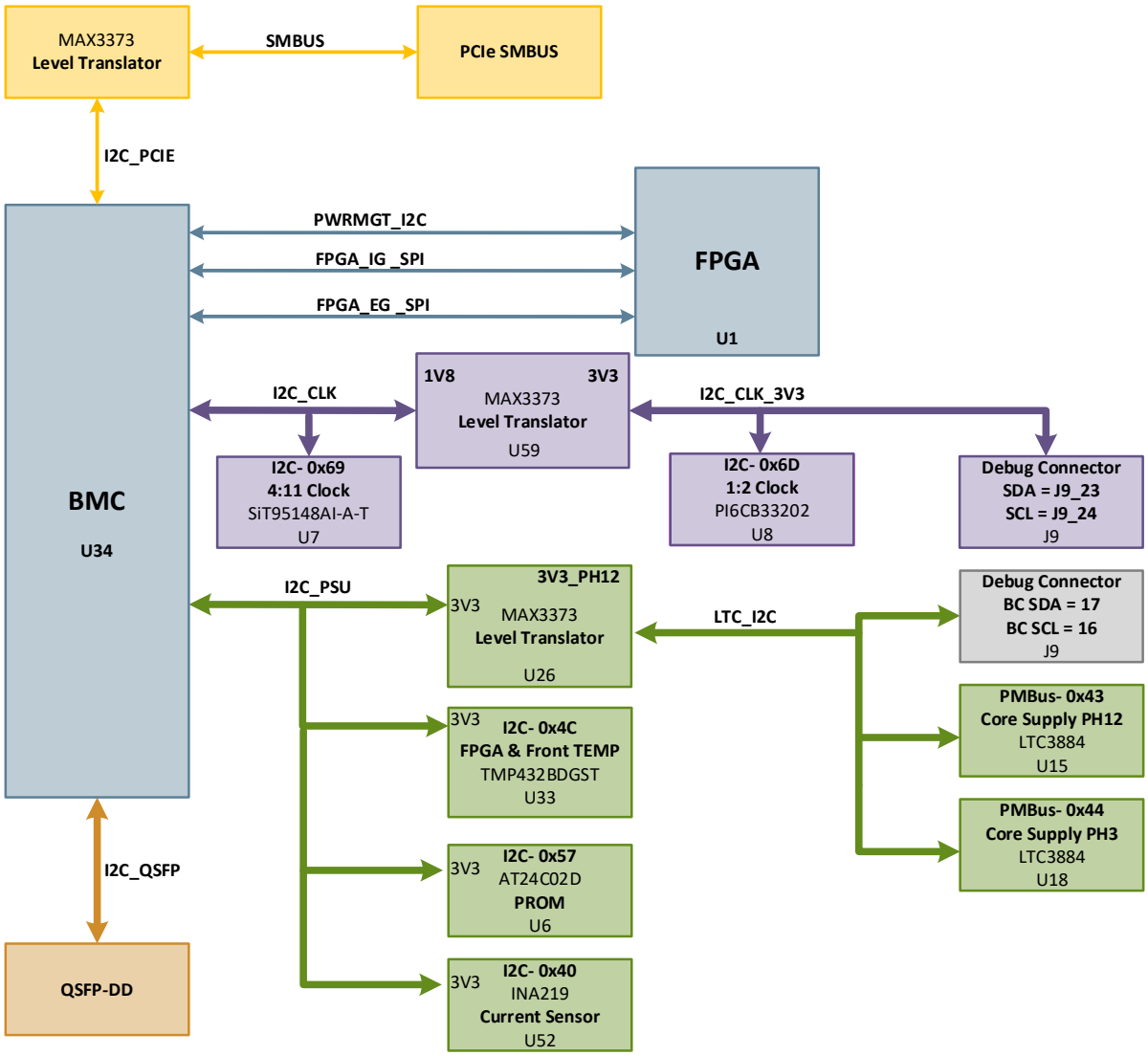


Table 16: FPGA-to-BMC I2C Signals

Signal Name	FPGA Pin
PWRMGT_SDA (SmartVID)	CY32
PWRMGT_SCL (SmartVID)	CU31

Table 17: I²C Addresses

Device	I²C Bus	I²C Address (hex)	Device Part Number	I2C Master	Accessible during System Standby (3.3V AUX powered)
EPROM BittWare ID PROM	FPGA - BMC	0x57	AT24C16C (16-Kbit – 2048 x 8)	BMC	No
PCIe clock buffer	BMC	0x6D	9DBL0242BKILFT	BMC	No
Main card clocks	BMC	0x69	SiT95148	BMC	No
Power controller	BMC	0x43, 0x44	LTC3884	BMC	No
Current monitor	BMC	0x40	INA219	BMC	No
Temperature sensor	BMC	0x4C	TMP432BDGST	BMC	No
QSFP-DD	FPGA - BMC		2027180100 (cage)	BMC	No

9.3.5 VPD EPROM

The EPROM is reserved for VPD (Vital Product Data) information and BittWare board information. The EPROM is programmed by BittWare at the time of shipment and then configured to be read-only. The I²C address for this chip is 0x57; see the “Device Addressing” section of the Atmel AT24C16C datasheet for further details.

The PROM is read-only. For customer production deployments, BittWare can pre-program customer-specific information in the reserved locations of the PROM or enable customers to write these locations.

Table 1 ID PROM Data

Address (hex)	Contents
0x57	BittWare fields
0x50-0x56	Reserved

9.3.6 FRU PROM (EEPROM)

The EEPROM is embedded in the BMC. The data format is defined in https://www.dmtf.org/sites/default/files/standards/documents/DSP0257_1.0.0.pdf.

9.4 SmartVID

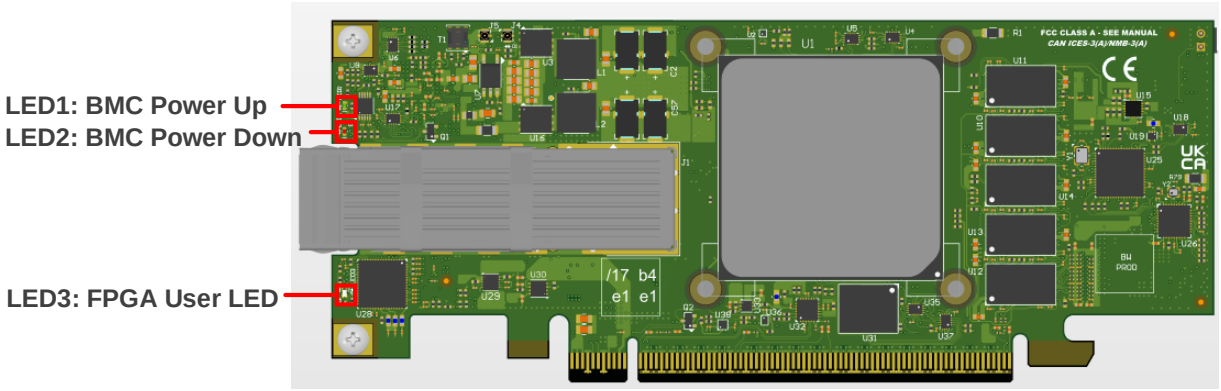
The Agilex FPGA on the IA-440i employs SmartVID to compensate for process variation by using voltage adaptation. The use of SmartVID is mandatory and requires certain entries in the Quartus Set-tings File (QSF). Please refer to the IA-440i *FPGA Developer Reference Guide* for details.

Intel Agilex Power Management User Guide:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/agilex/ug-ag-pwr.pdf

9.5 LEDs

The IA-440i has three LEDs. The BMC uses LED1 and LED2 for reporting its status, and the FPGA can drive LED3.

Figure 11: LED locations, top side of PCB



9.5.1 BMC Status LEDs

The two LEDs shown in the following table are either red or green and define the BMC behavior.

Table 18: BMC Status LEDs

LED Behavior Description	LED1 (GREEN)	LED2 (RED)
Power Start- at initial power-on	Blink @2Hz	Blink @2Hz
Power Off Ready- Board is powered off via the BMC	OFF	Blink @2Hz
Power On- Board is powered on and ready	Blink @2Hz	OFF
Power Off Fault- Fault on card and the BMC has powered down board supplies	OFF	Blink @2Hz
Power Off User- User manually powered down board supplies	ON	Blink @2Hz
Bootloader- User placed board into bootloader mode	OFF	Blink @0.5Hz
JTAG Mode- BMC is set up for JTAG programming	Blink @2Hz	Blink @2Hz
Factory Reset -Clears user FPGA and clock loads	Flash 2x	Flash 2x

9.5.2 FPGA User LEDs

The user has access to two LEDs driven directly from the FPGA. Table 19 lists the signal names for these User LEDs. Figure 11 shows their locations.

Table 19: FPGA User LEDs

LED	Signal	FPGA Pin	Color	Behavior
LED3	FPGA_LED_G FPGA_LED_R	DA19 CY20	Green Red	Active Low Active Low

9.6 Jumpers

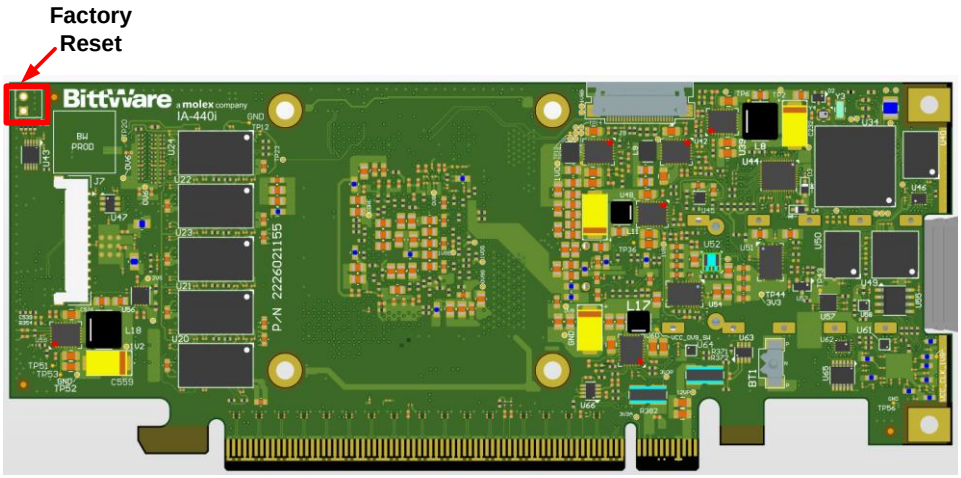
Jumpers on the IA-440i are for factory use only.

9.7 Factory Reset

To set the board back to its factory default,

1. Short the two J2 holes together using a jumper or equivalent,
2. Power cycle the card
3. Wait for the BMC to come up (should show Factory Reset LED pattern).
4. Remove the short from J2.

Figure 12: IA-440i Factory Reset.



10 USB

The IA-440i features multiple USB devices which are all accessible (through a USB hub) from the rear panel connector J7 connected to a BittWare accessory cable or breakout card (see 13 Accessories).

Note: For more information on deployment solutions in a BittWare TeraBox FPGA server, visit the TeraBox section on the BittWare website or contact your BittWare Sales representative for more information.

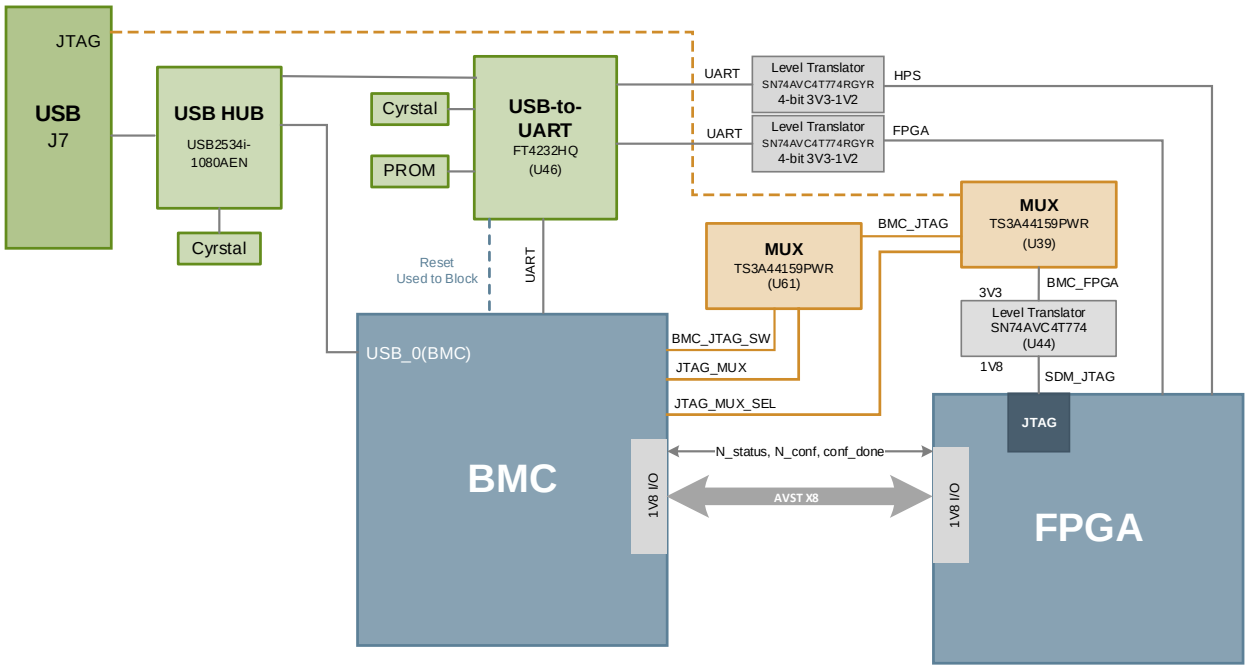
The USB connector gives access to the following USB devices:

1. Breakout header for external USB-Blaster pod access for JTAG access to the FPGA (see
2. BMC for access to control and status port (see BMC)
3. An FPGA user-controller UART

10.1 Board Features Accessible via USB

The USB port provides access to the BMC, USB UART, and USB Blaster (via external header). The USB connector is routed to the upstream port, a USB 2.0 hub, which in turn connects to the downstream devices. One downstream device is the BMC, which is a USB 2.0 compatible device . Secondly, an FTDI USB to UART converter provides a connection to the FPGA's UART interface and HPS UART.

Figure 13: USB Interface



10.1.1 USB-to-UART

The FPGA design can implement a UART which will be accessible through USB; the board features a FT234XD chip. Please download and install this chip's driver from the FTDI website.

FPGA pin name (QSF): RxD_UART_FPGA, TxD_UART_FPGA

10.2 USB and JTAG Connector

A Molex 504050-1291 Pico-Lock connector (J7) is used for the USB interface and external JTAG interface on the board. This connector is not part of the USB standard. See Accessories for cable and breakout card options for the IA-440i.

10.3 JTAG Utilities

The breakout card (see Accessories) and external header (J7) allows for external Intel Blaster pod access that provides access to the FPGA JTAG chain and allows you to reprogram the FPGA using the Quartus Programmer Tool. The user JTAG chain consists of the USB-to-JTAG device, through the BMC and to the FPGA. Note, the Intel blaster hardware is not included with the IA-440i.

Intel provides several other debug tools which use the JTAG chain:

- Signal Tap II Logic Analyzer
- Transceiver Toolkit
- External Memory Interface Toolkit
- In-System Sources and Probes Editor

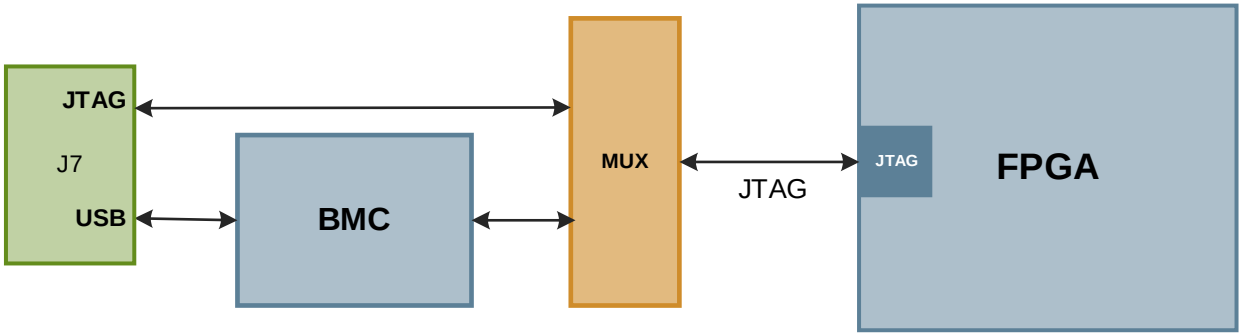
Refer to Intel's documentation for details on using these tools.

NOTE: for installation on Linux, refer to "Intel® FPGA Download Cable (formerly USB-Blaster) Driver for Linux" on the Intel website.

The Quartus installation folder includes the USB-Blaster II drivers.

10.3.1 JTAG Chain

Figure 14 JTAG Chain



JTAG debug access is only supported via Intel USB Blaster hardware.

10.3.2 USB-JTAG Connector

Connector J7 is a Pico-Lock connector that provides access to the FPGA JTAG chain using a BittWare breakout cable. See **Error! Reference source not found.** for cables and breakout card options for the IA-440i.

Table 20 USB-JTAG Connector Pinout

Pin	Signal
1	VCC_3V3
2	USB_IN_N
3	USB_IN_P
4	USB_GND_SHLD
5	GND
6	GND
7	VCC_3V
8	FT4232_TCk
9	FT4232_TDI
10	FT4232_TDO
11	FT4232_TMS
12	GND

11 Power

11.1 Power Specifications

The IA-440i board is designed to support a typical operating power consumption of 75W. The standard Fan/Heatsink COTS solution supports 75 Watts cooling with an ambient inlet temperature up to 35C. Under these conditions the FPGA die temperature will typically be kept below an operating junction temperature of 85C.

You can read the FPGA fabric temperature via the BMC and estimate the power required by the FPGA using Intel's EPE tool available on the Intel website.

11.2 Power Requirements

Power requirements for the IA-440i are application-specific. The card power draw might go from low, if the FPGA is unconfigured, to medium when the FPGA is programmed with an FPGA design. FPGA designs with high resource utilization, high toggle rate, and high clock frequency will increase the card power draw, which might approach the card's max power.

11.3 Power Sources

The IA-440i is powered from the host motherboard PCIe slot power supplies.

11.4 Power Monitoring

As noted in the Card Management section, the BMC monitors the power supplies in real time. You can use the SDK's BMC utility to read the values, or you can use MCTP/PLDM, as described in the *BMC Reference Guide for IA-440i*. The BMC Reference Guide also lists the sensors that the BMC is monitoring.

12 Mechanical

12.1 Chassis Requirements

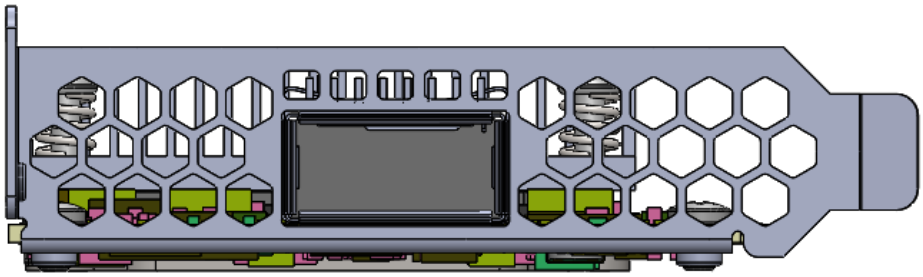
12.1.1 PCI Express

The IA-440i is capable of PCIe Gen5 with 16 lanes. The card requires a x16 PCIe slot for mechanical compatibility.

12.1.2 PCIe Bracket

The card ships with a low-profile PCIe faceplate bracket matching the card configuration. The example below shows the low-profile faceplate for a card configured with 1 QSFP-DD.

Figure 15: PCIe Faceplate

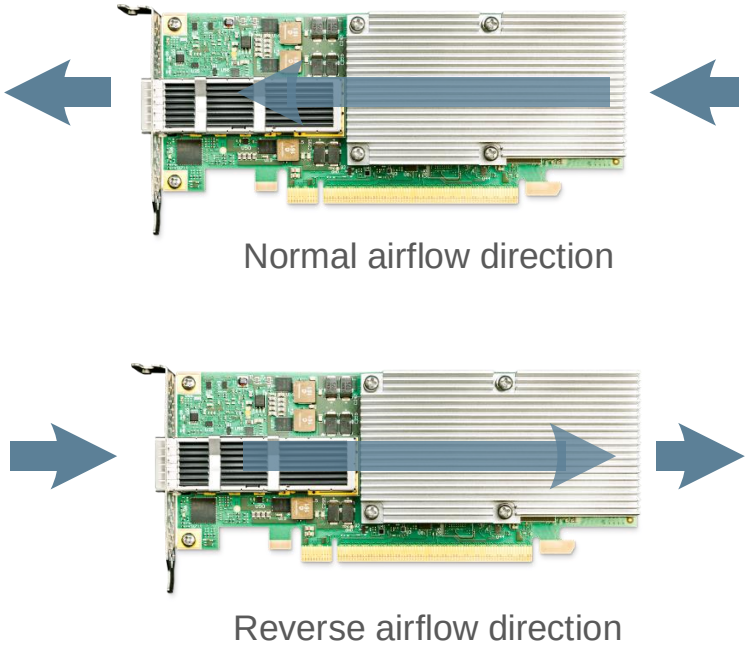


12.2 Air Flow

The IA-440i can be fitted with a passive heatsink. Be sure that the installation has sufficient airflow and that the power consumption is limited to keep the card within its operating temperature limits. The BMC monitors the FPGA temperature. Refer to your card's BMC Reference Guide for details.

Be sure to provide adequate cooling for the IA-440i using either of the two methods shown below.

Figure 16: IA-440i Airflow Methods



BittWare cards can operate at high temperatures depending on the power draw of the application in the FPGA. The Board Management Controller will power down the card to prevent damage if components reach above a certain temperature threshold. Monitor the temperature of your card to ensure it is running consistently within the supported temperature range. If the card powers down suddenly, this is often an indication that the BMC powered down due to overheating. BittWare recommends that you alter the card cooling to address this. The factors that affect the thermal performance of a card are:

- Power consumption of the card/FPGA
- Ambient temperature
- Airflow through the heatsink

Power consumption and ambient temperature are typically static. Therefore, if a card is overheating, BittWare recommends ensuring the chassis fans are oriented to blow through the card heatsink and suggests altering fan speed to increase airflow through the heatsink.

Note: BittWare has seen issues cooling cards in desktop and workstation environments. This is due to the typical placement of fans relative to the card heatsink. If a desktop chassis must be used, additional fans will likely be required to adequately cool the card. This can be additional chassis fans positioned to blow through the heatsink or standalone desk fans oriented to move air over the FPGA.

See BittWare's Lab and Open Bench Environment Card Cooling white paper for a how-to on BittWare's solution for cooling cards in an open-bench lab environment.

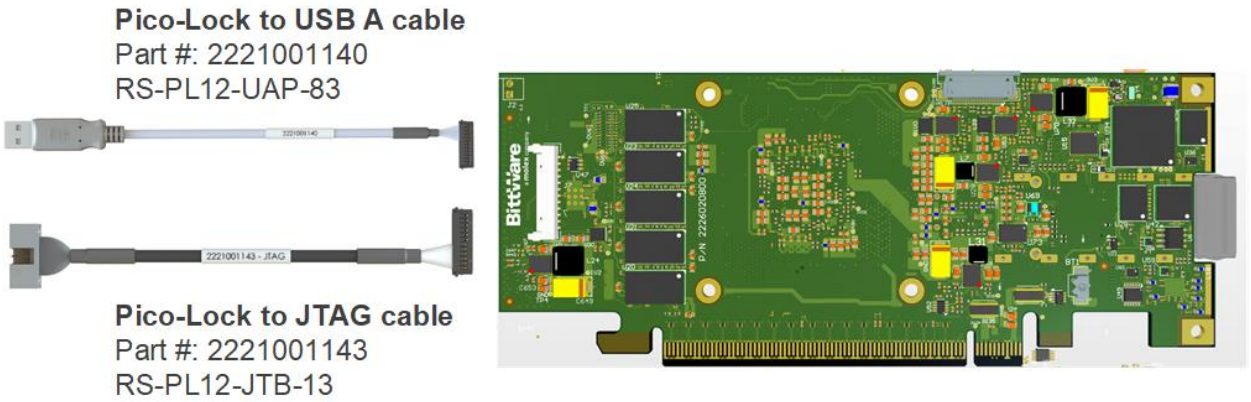
12.3 Card Dimensions

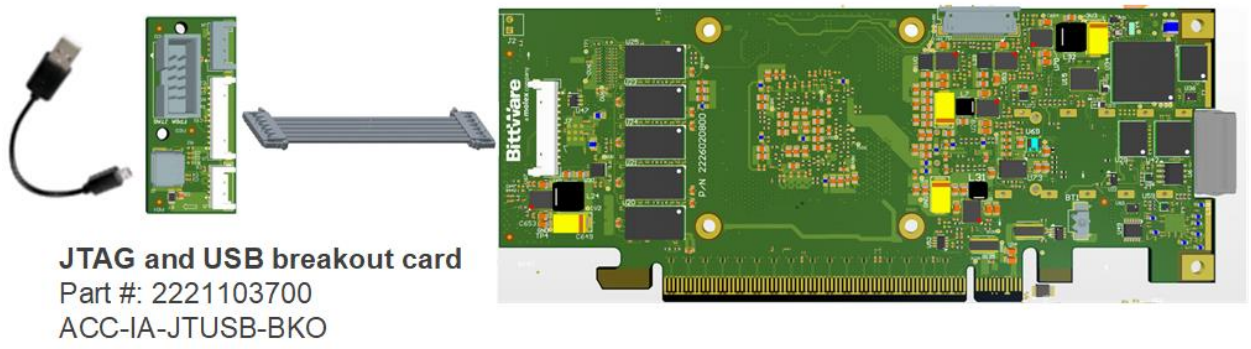
The IA-440i is a single width (98.4mm), half height (68.90 mm), low-profile form factor length (167.65mm) PCIe add-in card.

13 Accessories

Three accessories are available for the IA-440i as shown in Figure 17 below. The accessories are purchased separately and are **not** included with the card.

Figure 17: IA-440i Accessory Options





13.1 Pico-Lock to USB-A Cable

For **deployment**, BittWare recommends using a BittWare **Pico-Lock to USB A cable** which connects directly between the IA-440i and the host USB.

- **Part number**: 2221001140
- **Uses**:
  - Deployment
  - Accessing the BMC (FPGA programming, card health monitoring) ***This can also be done via PCIe***
  - Accessing the USB UART (FPGA UART and HPS UART)
- **Connects to**: J7 on the IA-440i

13.2 Pico-Lock to JTAG Cable

For **development**, you can purchase a custom BittWare Pico-Lock to JTAG cable that connects directly between the IA-440i and an Intel Blaster pod.

- **Part number**: 2221001143
- **Uses**:
  - Development and debug
  - Using the Intel Blaster pod[5] via the JTAG Interface
  - Programming the FPGA using the Quartus Programmer Tool
- **Connects to**: J7 on the IA-440i

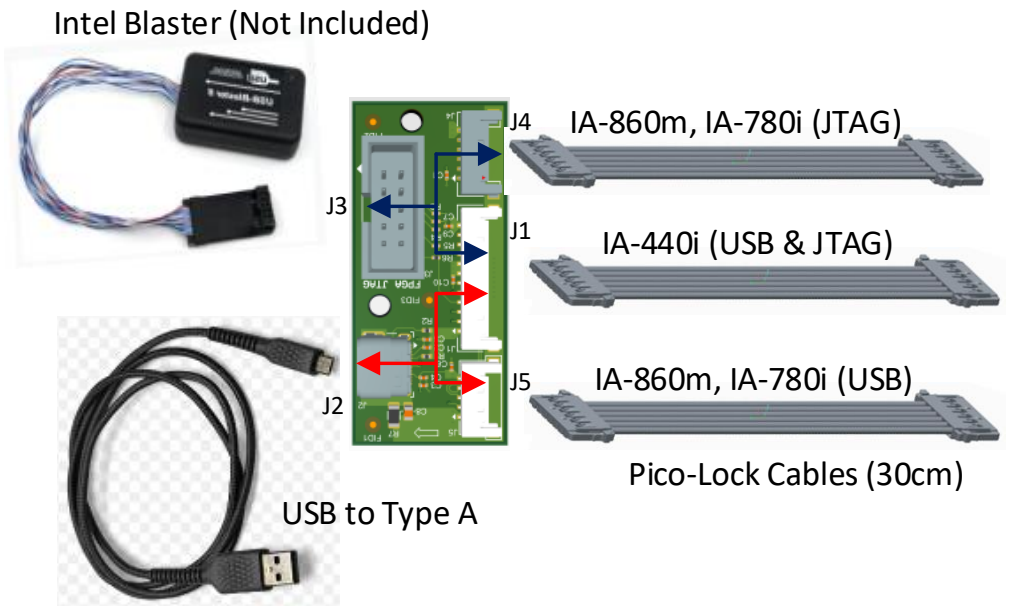
13.3 JTAG and USB Breakout Card

For **development**, BittWare recommends the IA-JTUSB-BREAKOUT card.

The IA-JTUSB-BREAKOUT card is used to program the FPGA on BittWare's Agilex I and M Series boards (IA-440i, IA-780i, IA-860m etc.). It is intended for use during development and allows you to program the FPGA via Intel's standard Blaster (or Blaster II) or via a USB connection to BittWare's Board Management Controller (BMC).

Figure 18 below shows an overview of the card. For complete information on the breakout card, refer to the IA-JTUSB-BREAKOUT Hardware Reference Guide.

Figure 18 IA-JTUSB-BREAKOUT Card Block Diagram



[5] The Intel Blaster is not included. For more information on Intel's FPGA download cables, see https://www.intel.com/content/www/us/en/products/details/fpga/development-kits/cables-adapters.html